Notice of References Cited	Application/Control No. 09/392,034	Applicant(s)/Patent Under Reexamination GONZALEZ ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5763932	06-1998	Pan et al.	257/510
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	S. Wolf, Silicon Processing for the VLSI Era, Process Integration. Vol. 2. Lattice Press 1990. pp. 54-55.
	V	A. Chatterjee et al., A Shallow Trench Isolation Using LOCOS Edge for Preventing Corner Effects for 0.25/0.18 Micron CMOS Technologies and Beyond. IEDM 1996, pp. 829-832.
	W	K. Ohe et al. Narrow-Width Effects of Shallow Trench Isolated CMOS with n+ Polysilicon Gate. IEEE 1989, pp. 1110-1116.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.